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CONFIDENTIAL COMMUNICATION

Date:	MAY 11, 2004
To:	EXAMINER KIMBERLY D. NGUYEN U.S. PATENT AND TRADEMARK OFFICE
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From: Phone #:	FRANK C. NICHOLAS (847) 424-2521
Client/Matter No.:	FR 000130 (7790/194)
# of Pages: (including cover sheet)	44

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TRANSMITTAL FORM

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Attorney Docket No.	FR 000130 (7790/194)
Application Number	10/015,965
Filing Date	NOVEMBER 30, 2001
First Named Inventor	YANNICK VINCENT
Group Art Unit	2876
Examiner	NGUYEN, KIMBERLY D

ENCLOSURES *(check all that apply)*

☐ Amendment	☐ Assignment Papers *(for an Application)*	☐ Appeal Communication to Board of Appeals and Interferences
☐ After Final	☐ Drawings	☒ Appeal Brief
☐ Affidavits/declaration(s)	☐ After Allowance Communication to Group	
	☐ Petition Routing Slip (PTO/SB/69) and Accompanying Petition	☐ Proprietary Information
☐ Status Letter	☐ To Convert a Provisional Application	☐ Post Card Receipt
☒ One-Month Petition for Extension of Time Request	☐ Power of Attorney, Revocation Change of Correspondence Address	☐ Additional Enclosure(s) *(please identify below)*
☐ Express Abandonment Request	☐ Terminal Disclaimer	☐
☐ Information Disclosure Statement, PTO-1449, an	☐ Small Entity Statement	☐
☐ Certified Copy of Priority Document(s)	☐ Request of Refund	☐
☐ Response to Missing Parts/ Incomplete Application		

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First Presentation of Multiple Dep Claim					+$145	—		+$290=	
					total add'l fee	$ 0		total add'l fee	$

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	FRANK C. NICHOLAS Registration No. 33,983 CARDINAL LAW GROUP 1603 Orrington Avenue, Suite 2000 Evanston, IL 60201
Signature	Date: May 11, 2004

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Signature	Date May 11, 2004
FRANK C. NICHOLAS (33,983)	

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- ☐ Certified Copy of Priority Document(s)
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CALCULATION OF FEE

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Total		Minus		0
Indep		Minus		0
First Presentation of Multiple Dep. Claim				

Small Entity			Large Entity	
Rate	Add'l Fee	or	Rate	Add'l Fee
x $9=	0		x $18=	
x $43	0		x $86	
+$145	---		+ $290=	
total add'l fee	$ 0		total add'l fee	$

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Individual name	FRANK C. NICHOLAS Registration No. 33,983 CARDINAL LAW GROUP 1603 Orrington Avenue, Suite 2000 Evanston, IL 60201
Signature	Date: May 11, 2004

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Date: May 11, 2004

OFFICIAL

PATENT
Case No. FR 000130
(7790/194)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

YANNICK VINCENT

Serial No.: 10/015,965

Filed: NOVEMBER 30, 2001

For: DATA-PROCESSING SYSTEM

Examiner: Nguyen, Kimberly D

Group Art Unit: 2876

APPEAL BRIEF

Mail Stop **Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant herewith respectfully presents its Brief on Appeal as follows:

1. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA. Koninklijke Philips Electronics N.V. is the ultimate parent of the assignee of record Philips Electronics North America Corporation, a Delaware corporation having an office and a place of business at 1251 Avenue of the Americas, New York, NY 10020-1104. Philips Electronics North America Corporation intends to further assign this application to Koninklijke Philips Electronics N.V.

2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-9 are currently pending in the application and are the claims on appeal. See, the Appendix. Claims 1, 3, 5, 7 and 9 stand finally rejected under 35 U.S.C. §102(b) as being anticipated by U S. Patent No. 6,574,776 to *Chiang*. Claims 2 and 6 stand finally rejected under 35 U S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent Publication No. 2003/0004891 to *Van Rensberg*. Claims 4 and 8 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent No. 5,978,822 to *Muwafi*.

4. STATUS OF AMENDMENTS

A reply under 37 C.F.R. §1.116 involving arguments supporting an allowance of claims 1-9 over *Chiang* and the remaining art of record was filed on 01/011/2004, but was not entered into the present application by Examiner Nguyen.

5. SUMMARY OF THE INVENTION

As illustrated in FIG. 1, the invention of the present application generally employs a microprocessor [PRC], a communication device [COM], and a hardware circuit [HARD]. In operation, communication device [COM] communicates with an electronic module [MOD] on behalf of microprocessor [PRCF] based on convention signal intended by electronic module [MOD] to be sent to microprocessor [PRC]. If the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE 1] is identical to the order of the bits of the word in the form of [BYTE2]. Similarly, if the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4]whereby the order of the bits of the word in the form of [BYTE 3] is identical to the order of the bits of the word in the form of [BYTE4]. Conversely, if the value of the convention

signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE2] are inverted with respect to the order of the bits of the word in the form of [BYTE1]. Similarly, if the value of the convention signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4] whereby the order of the bits of the word in the form of [BYTE4] are inverted with respect to the order of the bits of the word in the form of [BYTE3]. See, *U.S. Patent Application Serial No. 10/015,965* on page 4, line 5-26.

As illustrated in FIG. 4, for each bit of a word being transferred from electronic module [MOD] to microprocessor [PRC] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHMP], a right shift register [RXMP] electrically connected to switch [SWHMP] and a left shift register [RYMP] electrically connected to switch [SWHMP]. See, *U.S. Patent Application Serial No. 10/015,965* on page 5, line 23 to page 6, line 18.

As illustrated in FIG. 6, for each bit of a word being transferred from microprocessor [PRC] to electronic module [MOD] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHPM], a right shift register [RXPM] electrically connected to switch [SWHPM] and a left shift register [RYPM] electrically connected to switch [SWHPM]. See, *U S. Patent Application Serial No. 10/015,965* on page 7, line 18 to page 8, line 20.

6. ISSUE

Whether claims 1-9 are allowable over *Chiang*.

7. GROUPING OF CLAIMS

Claims 1-9 should be considered in two (2) groups.

Group I consists of claims 1-3 and 5-7, which are directed to a general embodiment of a hardware circuit for conditionally inverting, the order and/or value of bits of a word.

Group II consists of claims 4, 8 and 9, where are directed to a specific embodiment of the hardware circuit including a switch, a right shift register and a left shift register.

8. ARGUMENTS

Chiang. As illustrated in FIG 1, *Chiang* discloses a memory 11 electrically connected to a EDC processor unit 13 and a ECC-P- processor 15. In operation, a data block (e.g., 16 bits) is read from memory unit 11 and received by EDC processor unit 13 and ECC-P-parity processor unit 15, which also receives a processed form of the data block from EDC processor unit 13. See, *Chiang* at column 1, line 66 to column 2, line 30. Examiner Nguyen respectfully asserts that memory unit 11 is an electronic module as claimed in claims 1-9 and EDC processor unit 13 is the microprocessor claimed in claims 1-9 whereby electronic memory unit 11 intends to send a

convention signal to EDC processor unit 13 via a communication device as required by claims 1-9. However, a proper understanding of *Chiang* reveals that memory unit 11 only sends data blocks to EDC processor unit 13 as evidenced by the illustration of data exclusively being sent from memory unit 11 to EDC processor unit 13.

Furthermore, as illustrated in FIG. 7, *Chiang* further teaches EDC processor unit 13 accomplishes a EDC coding involving an inversion of EDC error detection bits d(k) by an EDC Bit Order Inverter. See, *Chiang* at column 5, line 7 to column 6, line 63. Nguyen respectfully asserts that EDC processor unit 13 uses Bit Order Inverter to invert the bits of the data block from memory 11 as a function of value of a convention signal. However, a proper understanding of *Chiang* reveals that (1) EDC Bit Order Inverter inverts EDC error detection bits d(k) from a left shift feedback register LSFR as opposed to the data block from memory unit 11, and (2) EDC Bit Order Inverter does not invert EDC error detection bits d(k) as a function of any signal as evidenced by the failure of Chiang to illustrate a signal being inputted into EDC Bit Order Inverter for purposes of controlling the inversion of EDC error detection bits d(k).

Claim Group 1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F 2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir

1989). The Appellant respectfully traverses the anticipation rejection of independent claims 1, 5 and 9, because *Chiang* fails to disclose and teaches away from the following limitations of independent claims 1, 5 and 9:

1. "a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor", and "a hardware circuit [HARD] allowing inversion or no inversion of the order of bits of a word as a function of the value of said convention signal during transfer of said word between the electronic module [MOD] and the microprocessor [PRC]" as recited in independent claims 1 and 5; and

2. "a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]", and "wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal" as recited in independent claim 9.

Withdrawal of the rejection of independent claims 1, 5 and 9 under 35 U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim 2 depends from independent claim 1. Therefore, dependent claim 2 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 2 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 2 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested.

Claim 3 depends from independent claim 1. Therefore, dependent claim 3 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 3 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim 6 depends from independent claim 5. Therefore, dependent claim 6 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 6 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 6 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested.

Claim 7 depends from independent claim 5. Therefore, dependent claim 7 includes all of the elements and limitations of independent claim 5 It is therefore respectfully submitted by the Applicant that dependent claim 7 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 7 under U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim Group II. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, MPEP §2143. The Appellant respectfully traverses this obviousness rejection of claims 4 and 8, because *Chiang* teaches away from "wherein said hardware circuit [HARD]includes: a switch [SWHMP, SWHPM]; a right shift register [RXMP, RYPM] electrically connected to said switch; and a left shift register [RYMP, RXPM] electrically connected to said switch" as recited in dependent claims 4 and 8. Specifically, *Chiang* teaches away from an incorporation of a switch within ED Bit Order Inverter by failing to teach a conditional inversion of the EDC error detection bits d(k) by the ED Bit Order Inverter.

Furthermore, claim 4 depends from independent claim 1. Therefore, dependent claim 4 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 4 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 4 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Claim 8 depends from independent claim 5. Therefore, dependent claim 8 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 8 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 8 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Dated: **May 11, 2004**

Respectfully submitted,
YANNICK VINCENT

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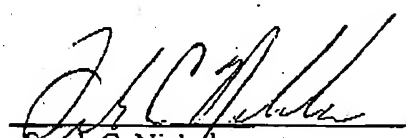

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Frank C. Nicholas
Registration No. 33,983
Attorney for Appellant

APPENDIX

1. A data-processing system, comprising:

a microprocessor [PRC];

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].

---

2. The data-processing system as claimed in claim 1, wherein said electronic module [MOD] is a Subscriber Identity Module card.

3 The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.

4 The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] includes:

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

5. A terminal, comprising:

a microprocessor [PRC];

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].

6. The terminal as claimed in claim 5, wherein said electronic module [MOD] is a Subscriber Identity Module card

7 The terminal as claimed in claim 5, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.

8. The terminals as claimed in claim 5, wherein said hardware circuit [HARD]includes:

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

9. A data-processing system, comprising:

a hardware circuit [HARD];

a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and

wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal.

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(Date of Deposit)

FRANK C. NICHOLAS (33,083)
Name of Appellant, assignee or registered representative

Signature

May 11, 2004
Date of Signature

PATENT
Case No. FR 000130
(7790/194)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of)
)
YANNICK VINCENT)
) Examiner: Nguyen, Kimberly D
Serial No.: 10/015,965)
) Group Art Unit: 2876
Filed NOVEMBER 30, 2001)
)
For: DATA-PROCESSING SYSTEM)

APPEAL BRIEF

Mail Stop **Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant herewith respectfully presents its Brief on Appeal as follows:

1. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA. Koninklijke Philips Electronics N.V. is the ultimate parent of the assignee of record Philips Electronics North America Corporation, a Delaware corporation having an office and a place of business at 1251 Avenue of the Americas, New York, NY 10020-1104. Philips Electronics North America Corporation intends to further assign this application to Koninklijke Philips Electronics N.V.

2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal.

3. STATUS OF CLAIMS

Claims 1-9 are currently pending in the application and are the claims on appeal. See, the Appendix. Claims 1, 3, 5, 7 and 9 stand finally rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,574,776 to *Chiang*. Claims 2 and 6 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent Publication No. 2003/0004891 to *Van Rensberg*. Claims 4 and 8 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent No. 5,978,822 to *Muwafi*

4. STATUS OF AMENDMENTS

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5. SUMMARY OF THE INVENTION

As illustrated in FIG. 1, the invention of the present application generally employs a microprocessor [PRC], a communication device [COM], and a hardware circuit [HARD]. In operation, communication device [COM] communicates with an electronic module [MOD] on behalf of microprocessor [PRCF] based on convention signal intended by electronic module [MOD] to be sent to microprocessor [PRC]. If the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE 1] is identical to the order of the bits of the word in the form of [BYTE2]. Similarly, if the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4]whereby the order of the bits of the word in the form of [BYTE 3] is identical to the order of the bits of the word in the form of [BYTE4]. Conversely, if the value of the convention

signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE2] are inverted with respect to the order of the bits of the word in the form of [BYTE1] Similarly, if the value of the convention signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4] whereby the order of the bits of the word in the form of [BYTE4] are inverted with respect to the order of the bits of the word in the form of [BYTE3]. See, *U.S Patent Application Serial No. 10/015,965* on page 4, line 5-26.

As illustrated in FIG. 4, for each bit of a word being transferred from electronic module [MOD] to microprocessor [PRC] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHMP], a right shift register [RXMP] electrically connected to switch [SWHMP] and a left shift register [RYMP] electrically connected to switch [SWHMP]. See, *U.S Patent Application Serial No. 10/015,965* on page 5, line 23 to page 6, line 18.

As illustrated in FIG. 6, for each bit of a word being transferred from microprocessor [PRC] to electronic module [MOD] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHPM], a right shift register [RXPM] electrically connected to switch [SWHPM] and a left shift register [RYPM] electrically connected to switch [SWHPM]. See, *U.S. Patent Application Serial No. 10/015,965* on page 7, line 18 to page 8, line 20.

6. ISSUE

Whether claims 1-9 are allowable over *Chiang*.

7. GROUPING OF CLAIMS

Claims 1-9 should be considered in two (2) groups.

Group I consists of claims 1-3 and 5-7, which are directed to a general embodiment of a hardware circuit for conditionally inverting, the order and/or value of bits of a word.

Group II consists of claims 4, 8 and 9, where are directed to a specific embodiment of the hardware circuit including a switch, a right shift register and a left shift register.

8. ARGUMENTS

Chiang. As illustrated in FIG. 1, *Chiang* discloses a memory 11 electrically connected to a EDC processor unit 13 and a ECC-P- processor 15. In operation, a data block (e g., 16 bits) is read from memory unit 11 and received by EDC processor unit 13 and ECC-P-parity processor unit 15, which also receives a processed form of the data block from EDC processor unit 13. See, *Chiang* at column 1, line 66 to column 2, line 30. Examiner Nguyen respectfully asserts that memory unit 11 is an electronic module as claimed in claims 1-9 and EDC processor unit 13 is the microprocessor claimed in claims 1-9 whereby electronic memory unit 11 intends to send a

convention signal to EDC processor unit 13 via a communication device as required by claims 1-9. However, a proper understanding of *Chiang* reveals that memory unit 11 only sends data blocks to EDC processor unit 13 as evidenced by the illustration of data exclusively being sent from memory unit 11 to EDC processor unit 13.

Furthermore, as illustrated in FIG. 7, *Chiang* further teaches EDC processor unit 13 accomplishes a EDC coding involving an inversion of EDC error detection bits d(k) by an EDC Bit Order Inverter. See, *Chiang* at column 5, line 7 to column 6, line 63. Nguyen respectfully asserts that EDC processor unit 13 uses Bit Order Inverter to invert the bits of the data block from memory 11 as a function of value of a convention signal. However, a proper understanding of *Chiang* reveals that (1) EDC Bit Order Inverter inverts EDC error detection bits d(k) from a left shift feedback register LSFR as opposed to the data block from memory unit 11, and (2) EDC Bit Order Inverter does not invert EDC error detection bits d(k) as a function of any signal as evidenced by the failure of Chiang to illustrate a signal being inputted into EDC Bit Order Inverter for purposes of controlling the inversion of EDC error detection bits d(k).

Claim Group 1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim " *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir.

1989). The Appellant respectfully traverses the anticipation rejection of independent claims 1, 5 and 9, because *Chiang* fails to disclose and teaches away from the following limitations of independent claims 1, 5 and 9:

1. "a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor", and "a hardware circuit [HARD] allowing inversion or no inversion of the order of bits of a word as a function of the value of said convention signal during transfer of said word between the electronic module [MOD] and the microprocessor [PRC]" as recited in independent claims 1 and 5; and

2. "a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]", and "wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal" as recited in independent claim 9

Withdrawal of the rejection of independent claims 1, 5 and 9 under 35 U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim 2 depends from independent claim 1. Therefore, dependent claim 2 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 2 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 2 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested.

Claim 3 depends from independent claim 1. Therefore, dependent claim 3 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 3 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim 6 depends from independent claim 5. Therefore, dependent claim 6 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 6 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 6 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested.

Claim 7 depends from independent claim 5. Therefore, dependent claim 7 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 7 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 7 under U.S.C §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim Group II. To establish a *prima facie* case of obviousness, three basic criteria must be met First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. See, MPEP §2143. The Appellant respectfully traverses this obviousness rejection of claims 4 and 8, because *Chiang* teaches away from "wherein said hardware circuit [HARD]includes: a switch [SWHMP, SWHPM]; a right shift register [RXMP, RYPM] electrically connected to said switch; and a left shift register [RYMP, RXPM] electrically connected to said switch" as recited in dependent claims 4 and 8. Specifically, *Chiang* teaches away from an incorporation of a switch within ED Bit Order Inverter by failing to teach a conditional inversion of the EDC error detection bits d(k) by the ED Bit Order Inverter.

Furthermore, claim 4 depends from independent claim 1. Therefore, dependent claim 4 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 4 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 4 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Claim 8 depends from independent claim 5. Therefore, dependent claim 8 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 8 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 8 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Dated May 11, 2004

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APPENDIX

1 A data-processing system, comprising:

a microprocessor [PRC];

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor, and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC]

2. The data-processing system as claimed in claim 1, wherein said electronic module [MOD] is a Subscriber Identity Module card.

3. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.

4. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] includes

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

5. A terminal, comprising:

a microprocessor [PRC];

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].

---

6 The terminal as claimed in claim 5, wherein said electronic module [MOD] is a Subscriber Identity Module card

7. The terminal as claimed in claim 5, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal.

8. The terminals as claimed in claim 5, wherein said hardware circuit [HARD]includes:

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

9 A data-processing system, comprising:

a hardware circuit [HARD];

a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and

wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal.

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(Date of Deposit)

FRANK C. NICHOLAS (33,983)
Name of Appellant, assignee, or registered representative

Signature

May 11, 2004
Date of Signature

PATENT
Case No. FR 000130
(7790/194)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:
YANNICK VINCENT

Serial No : 10/015,965

Filed NOVEMBER 30, 2001

For. DATA-PROCESSING SYSTEM

Examiner: Nguyen, Kimberly D

Group Art Unit: 2876

APPEAL BRIEF

Mail Stop **Appeal Brief - Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant herewith respectfully presents its Brief on Appeal as follows:

1. REAL PARTY IN INTEREST

The real party in interest is Koninklijke Philips Electronics N.V., a corporation of The Netherlands having an office and a place of business at Groenewoudseweg 1, Eindhoven, Netherlands 5621 BA. Koninklijke Philips Electronics N.V. is the ultimate parent of the assignee of record Philips Electronics North America Corporation, a Delaware corporation having an office and a place of business at 1251 Avenue of the Americas, New York, NY 10020-1104. Philips Electronics North America Corporation intends to further assign this application to Koninklijke Philips Electronics N.V

2. RELATED APPEALS AND INTERFERENCES

Appellant and the undersigned attorney are not aware of any other appeals or interferences which will directly affect or be directly affected by or having a bearing on the Board's decision in the pending appeal

3. STATUS OF CLAIMS

Claims 1-9 are currently pending in the application and are the claims on appeal. See, the Appendix Claims 1, 3, 5, 7 and 9 stand finally rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 6,574,776 to *Chiang*. Claims 2 and 6 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U.S. Patent Publication No. 2003/0004891 to *Van Rensberg* Claims 4 and 8 stand finally rejected under 35 U.S.C. §103(a) as being unpatentable over *Chiang* in view of U S. Patent No. 5,978,822 to *Muwafi*.

4. STATUS OF AMENDMENTS

A reply under 37 C.F.R. §1.116 involving arguments supporting an allowance of claims 1-9 over *Chiang* and the remaining art of record was filed on 01/011/2004, but was not entered into the present application by Examiner Nguyen.

5. SUMMARY OF THE INVENTION

As illustrated in FIG. 1, the invention of the present application generally employs a microprocessor [PRC], a communication device [COM], and a hardware circuit [HARD]. In operation, communication device [COM] communicates with an electronic module [MOD] on behalf of microprocessor [PRCF] based on convention signal intended by electronic module [MOD] to be sent to microprocessor [PRC]. If the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE 1] is identical to the order of the bits of the word in the form of [BYTE2]. Similarly, if the value of the convention signal is "0", then hardware circuit [HARD] does not invert the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4]whereby the order of the bits of the word in the form of [BYTE 3] is identical to the order of the bits of the word in the form of [BYTE4]. Conversely, if the value of the convention

signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during a transfer of the word from electronic module [MOD] to microprocessor [PRC] via communication device [COM] in the form of [BYTE1] and [BYTE2] whereby the order of the bits of the word in the form of [BYTE2] are inverted with respect to the order of the bits of the word in the form of [BYTE1]. Similarly, if the value of the convention signal is "1", then hardware circuit [HARD] inverts the order of the bits of a word during the transfer a word from microprocessor [PRC] to electronic module [MOD] via communication device [COM] in the form of [BYTE3] and [BYTE4] whereby the order of the bits of the word in the form of [BYTE4] are inverted with respect to the order of the bits of the word in the form of [BYTE3]. See, *U.S. Patent Application Serial No. 10/015,965* on page 4, line 5-26.

As illustrated in FIG. 4, for each bit of a word being transferred from electronic module [MOD] to microprocessor [PRC] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHMP], a right shift register [RXMP] electrically connected to switch [SWHMP] and a left shift register [RYMP] electrically connected to switch [SWHMP] See, *U.S. Patent Application Serial No. 10/015,965* on page 5, line 23 to page 6, line 18.

As illustrated in FIG. 6, for each bit of a word being transferred from microprocessor [PRC] to electronic module [MOD] via communication circuit [COM], hardware circuit [HARD] specifically employs a switch [SWHPM], a right shift register [RXPM] electrically connected to switch [SWHPM] and a left shift register [RYPM] electrically connected to switch [SWHPM]. See, *U S Patent Application Serial No. 10/015,965* on page 7, line 18 to page 8, line 20.

6. ISSUE

Whether claims 1-9 are allowable over *Chiang*.

7. GROUPING OF CLAIMS

Claims 1-9 should be considered in two (2) groups

Group I consists of claims 1-3 and 5-7, which are directed to a general embodiment of a hardware circuit for conditionally inverting, the order and/or value of bits of a word.

Group II consists of claims 4, 8 and 9, where are directed to a specific embodiment of the hardware circuit including a switch, a right shift register and a left shift register.

8. ARGUMENTS

Chiang. As illustrated in FIG. 1, *Chiang* discloses a memory 11 electrically connected to a EDC processor unit 13 and a ECC-P- processor 15. In operation, a data block (e.g., 16 bits) is read from memory unit 11 and received by EDC processor unit 13 and ECC-P-parity processor unit 15, which also receives a processed form of the data block from EDC processor unit 13. See, *Chiang* at column 1, line 66 to column 2, line 30. Examiner Nguyen respectfully asserts that memory unit 11 is an electronic module as claimed in claims 1-9 and EDC processor unit 13 is the microprocessor claimed in claims 1-9 whereby electronic memory unit 11 intends to send a

convention signal to EDC processor unit 13 via a communication device as required by claims 1-9. However, a proper understanding of *Chiang* reveals that memory unit 11 only sends data blocks to EDC processor unit 13 as evidenced by the illustration of data exclusively being sent from memory unit 11 to EDC processor unit 13.

Furthermore, as illustrated in FIG. 7, *Chiang* further teaches EDC processor unit 13 accomplishes a EDC coding involving an inversion of EDC error detection bits d(k) by an EDC Bit Order Inverter. See, *Chiang* at column 5, line 7 to column 6, line 63. Nguyen respectfully asserts that EDC processor unit 13 uses Bit Order Inverter to invert the bits of the data block from memory 11 as a function of value of a convention signal. However, a proper understanding of *Chiang* reveals that (1) EDC Bit Order Inverter inverts EDC error detection bits d(k) from a left shift feedback register LSFR as opposed to the data block from memory unit 11, and (2) EDC Bit Order Inverter does not invert EDC error detection bits d(k) as a function of any signal as evidenced by the failure of Chiang to illustrate a signal being inputted into EDC Bit Order Inverter for purposes of controlling the inversion of EDC error detection bits d(k).

Claim Group 1. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). "The identical invention must be shown in as complete detail as is contained in the ... claim." *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 USPQ2d 1913, 1920 (Fed. Cir.

1989). The Appellant respectfully traverses the anticipation rejection of independent claims 1, 5 and 9, because *Chiang* fails to disclose and teaches away from the following limitations of independent claims 1, 5 and 9:

1 "a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor", and "a hardware circuit [HARD] allowing inversion or no inversion of the order of bits of a word as a function of the value of said convention signal during transfer of said word between the electronic module [MOD] and the microprocessor [PRC]" as recited in independent claims 1 and 5; and

2 "a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]", and "wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal" as recited in independent claim 9.

Withdrawal of the rejection of independent claims 1, 5 and 9 under 35 U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested

Claim 2 depends from independent claim 1. Therefore, dependent claim 2 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 2 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 2 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested

Claim 3 depends from independent claim 1. Therefore, dependent claim 3 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 3 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 1 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim 6 depends from independent claim 5. Therefore, dependent claim 6 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 6 is allowable over *Chiang* in view of *Van Rensberg* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 6 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Van Rensberg* is therefore respectfully requested

Claim 7 depends from independent claim 5. Therefore, dependent claim 7 includes all of the elements and limitations of independent claim 5 It is therefore respectfully submitted by the Applicant that dependent claim 7 is allowable over *Chiang* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 7 under U.S.C. §102(b) as being anticipated by *Chiang* is therefore respectfully requested.

Claim Group II. To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations See, MPEP §2143. The Appellant respectfully traverses this obviousness rejection of claims 4 and 8, because *Chiang* teaches away from "wherein said hardware circuit [HARD]includes a switch [SWHMP, SWHPM]; a right shift register [RXMP, RYPM] electrically connected to said switch; and a left shift register [RYMP, RXPM] electrically connected to said switch" as recited in dependent claims 4 and 8. Specifically, *Chiang* teaches away from an incorporation of a switch within ED Bit Order Inverter by failing to teach a conditional inversion of the EDC error detection bits d(k) by the ED Bit Order Inverter.

Furthermore, claim 4 depends from independent claim 1 Therefore, dependent claim 4 includes all of the elements and limitations of independent claim 1. It is therefore respectfully submitted by the Applicant that dependent claim 4 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 4 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 3 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Claim 8 depends from independent claim 5 . Therefore, dependent claim 8 includes all of the elements and limitations of independent claim 5. It is therefore respectfully submitted by the Applicant that dependent claim 8 is allowable over *Chiang* in view of *Muwafi* for at least the same reason as set forth herein with respect to independent claim 5 being allowable over *Chiang*. Withdrawal of the rejection of dependent claim 8 under U.S.C. §103(a) as being unpatentable over *Chiang* in view of *Muwafi* is therefore respectfully requested.

Dated May 11, 2004

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APPENDIX

1. A data-processing system, comprising

a microprocessor [PRC],

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC].

2. The data-processing system as claimed in claim 1, wherein said electronic module [MOD] is a Subscriber Identity Module card.

3. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal

4. The data-processing system as claimed in claim 1, wherein said hardware circuit [HARD] includes:

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

5. A terminal, comprising:

a microprocessor [PRC];

a communication device [COM] communicating with an electronic module [MOD] intended to send a convention signal to said microprocessor; and

a hardware circuit [HARD] allowing an inversion of an order of bits of a word as a function of a value of the convention signal during a transfer of the word between said electronic module [MOD] and said microprocessor [PRC]

---

6 The terminal as claimed in claim 5, wherein said electronic module [MOD] is a Subscriber Identity Module card.

7 The terminal as claimed in claim 5, wherein said hardware circuit [HARD] allows inversion of the value of the bits of the word as a function of the value of the convention signal

8. The terminals as claimed in claim 5, wherein said hardware circuit [HARD]includes:

a switch [SWHMP, SWHPM];

a right shift register [RXMP, RYPM] electrically connected to said switch; and

a left shift register [RYMP, RXPM] electrically connected to said switch.

9. A data-processing system, comprising:

a hardware circuit [HARD];

a communication device [COM] for communicating a contention signal and a word to said hardware circuit [HARD] from one of a microprocessor [PRC] and an electronic module [MOD]; and

wherein said hardware circuit includes means for implementing one of a direct convention and an indirect convention of an order of bits of the word as a function of a value of the convention signal.